REMARKS

I. Introduction

Applicants appreciate the Examiner's withdrawal of the objections to the claims and drawings. With respect to the prior art rejections, Applicants respectfully submit that the claims are patentable over the cited art and that the current rejections should be withdrawn, for the reasons set forth below.

II. Independent Claims 1 and 44

Independent Claims 1 and 44 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,831,989 to Fujisaki. A rejection of a claim under 35 U.S.C. § 102(b) requires that a single reference contain each and every element recited in the claim. Applicants respectfully request withdrawal of the rejections against independent Claims 1 and 44 (and their dependent claims) because, as admitted by the Examiner, Fujisaki does not teach each and every element recited in those claims. Also, Applicants respectfully submit that one skilled in the art would not have been motivated to modify Fujisaki as suggested by the Examiner.

A. The Examiner Has Admitted that Fujisaki Does Not Anticipate the Claims

Independent Claims 1 and 44 recite a memory array comprising a primary block of memory cells and storing a flag in a set of memory cells in the memory array that is allocated to the primary block in response to an error in writing to the primary block. This is not shown in Fujisaki. Fujisaki is directed to a testing apparatus for a memory array (the "memory under test (MUT)"). Figure 6 shows that the MUT has a main memory cell array (the purported primary block) and row and column address relief lines (the purported redundant block). The testing apparatus is "built around" the MUT and contains a failure analysis memory 5 that is separate from the MUT. Fujisaki teaches writing a logical 1 (the purported flag) in the failure analysis

memory 5 when the testing apparatus finds a failure in the MUT. As is clearly shown in Figure 5 and described in Fujisaki, the failure analysis memory 5 is not part of the MUT. Accordingly, the purported flag in Fujisaki is not stored in the same memory array that contains the primary block, as required by Claims 1 and 44.

The Examiner admitted this deficiency in his Response to Arguments in the present Office Action by admitting that Fujisaki needs to be modified to yield the claimed invention:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine or make integral Fujisaki's failure analysis memory and MUT, since it would have been held that forming in one piece an article which has formerly been formed in two pieces and put together only involves routine skill in the art. . . . It is the Examiner's conclusion that independent claims 1 and 44 are not patentably distinct or non-obvious over the prior art of record, names Fujisaki (US-5831989). Therefore, the [35 U.S.C. § 102(b)] rejection is maintained.

Contrary to the Examiner's assertion, Applicants respectfully submit that the 35 U.S.C. § 102(b) rejection cannot be maintained because the Examiner is using an obviousness argument to maintain the anticipation rejection. Accordingly, Applicants respectfully request removal of the rejection against independent Claims 1 and 44 and their dependent claims.

B. One Skilled in the Art Would Not Have Been Motivated to Modify Fujisaki as Suggested in the Office Action

Even if independent Claims 1 and 44 had been rejected under 35 U.S.C. § 103(a) instead 35 U.S.C. § 102(b), Applicants respectfully submit that the rejections would still need to be withdrawn because one skilled in the art would not have been motivated to modify Fujisaki as proposed in the Office Action. In the Office Action, the Examiner pointed out that page 5, lines 8-10 of Applicants' specification state that "instead of being part of the same memory array 50, the primary and redundant memory arrays 52, 54 can be separated into two or more memory arrays." However, it is a well-known axiom of patent law that an Examiner cannot use an

applicant's specification as a blueprint to architect a rejection using hindsight reconstruction. The question is not whether one skilled in the art would have been motivated to modify Fujisaki after reading Applicants' specification, but rather whether one skilled in the art would have been motivated to modify Fujisaki to yield the claimed invention ***at the time the invention was made.***

It was also asserted in the Office Action that combining Fujisaki's failure analysis memory and the MUT would have been obvious because forming, in one piece, an article that has formerly been formed in two pieces involves only routine skill in the art. However, one skilled in the art would not have been motivated to make such a combination because the combination would alter the basic operating principal of the reference and, possibly, make the reference inoperable. See MPEP 2143.01. In Fujisaki, the failure analysis memory is a part of a memory testing apparatus that is used to test a MUT. It is important for the failure analysis memory to be able to reliably store data, as the data stored in the failure analysis memory is used to determine whether or not relief of the MUT is possible using its redundant memory. Because of the importance of using reliable memory, Applicants respectfully submit that one skilled in the art would not have been motivated to use untested memory cells in the MUT as the failure analysis memory because such memory cells have not yet been proven reliable. The whole point of testing the MUT is to determine whether that memory can reliably store data. Using memory cells in the MUT to store data needed to make this determination subjects the determination to the very flaws that the testing is designed to detect. Therefore, under the proposed modification, not only would the basic operating principle of the memory testing apparatus be altered (from using a memory of known reliability to using a memory of unknown reliability), but it could also result in making the memory testing apparatus inoperable (if the memory testing apparatus can not longer reliably test the MUT because bad memory cells in the MUT are used to store the

failure analysis data). For these reasons, Applicants respectfully submit that one skilled in the art would not have been motivated to modify Fujisaki as proposed in the Office Action.

III. Independent Claim 18

Independent Claim 18 was rejected under 35 U.S.C. § 102(b) as being anticipated by Fujisaki. Independent Claim 18 recites "while attempting to write to the primary block, determining that an error occurred in writing to the primary block." Applicants respectfully request withdrawal of the rejections against independent Claim 18 (and its dependent claims) because the Examiner has admitted that Fujisaki does not teach this element.

As explained in Applicants' last amendment, pages 8-9 of Applicants' specification describe two approaches to determining whether an error occurred in writing to memory. In the first approach, data is written to memory, a separate read operation is used to read the stored data out of the memory, and the read data is compared with the data expected to be stored in the memory. Accordingly, the first approach involves writing to a memory cell then reading the cell that was just written to to compare the values. In the second approach, instead of writing, reading, and then comparing, an error is determined ***while attempting to write to the memory***. The second approach avoids the overhead associated with the first approach of switching from a write voltage condition to a read voltage condition to determine whether an error occurred. Independent Claim 18 is directed to the second approach, while Fujisaki uses the first approach.

The Response to Arguments section in the present Office Action states that "the Examiner asserts that Fujisaki teaches the [sic] writing-then-reading the cell that was just written to." In other words, the Examiner agrees with Applicants that Fujisaki teaches the first approach discussed above and not the second approach, which is claimed in Claim 18. Accordingly, the 35

U.S.C. § 102(b) rejections against independent Claim 18 and its dependent claims should be removed.

Applicants would now like to address some additional points raised by the Examiner. The Examiner pointed out that Fujisaki teaches, "during a test of a memory under test MUT," writing a logical "1" indicating failure of a memory cell. The phrase "during a test of a memory under test MUT" does not teach determining that an error occurred in writing to the primary block ***"while attempting to write to the primary block,"*** as claimed in Claim 18. Instead, "during a test of a memory under test MUT" refers to "writing-then-reading a cell that was just written to," as admitted by the Examiner. Also, the Examiner appears to be ignoring the recited limitation of "while attempting to write to the primary block" in Claim 18. The Examiner stated that he is interpreting "while attempting to write to the primary block, determining that an error occurred in writing to the primary block" to cover any situation in which the value of a memory cell is read to determine if an error occurred in writing to the cell. Applicants respectfully submit that the claim limitation must be given weight and cannot be ignored simply because the applied reference does not meet the limitation.

Applicants also note that, as with independent Claims 1 and 44, the Examiner has further admitted that Fujisaki does not anticipate independent Claim 18 by relying on obviousness arguments to support the anticipation rejection. See page 4 ("independent claim 18 is not patentably distinct or non-obvious over the prior art of record namely, Fujisaki (US-5831989).").

In view of the above remarks, Applicants respectfully submit that the rejections of independent Claim 18 and its dependent claims should be withdrawn.

IV. Independent Claim 36

Independent Claim 36 recites "a three-dimensional memory array of vertically-stacked field-programmable memory cells" and was rejected under 35 U.S.C. § 103(a) as being unpatentable over the proposed combination of Fujisaki and U.S. Patent No. 5,278,839 to Matsumoto et al. In the Response to Arguments section in the present Office Action, the Examiner admitted that neither Fujisaki nor Matsumoto et al. teaches a three-dimensional memory array. However, the Examiner asserted that using a three-dimensional memory array of vertically-stacked field-programmable memory cells is merely a design choice and cannot constitute patentability. Applicants respectfully disagree. At the very minimum, the Examiner needs to provide a reference that teaches the recited "three-dimensional memory array of vertically-stacked field-programmable memory cells" and offer a motivation as to why one skilled in the art would have been motivated to replace the memory arrays disclosed in Fujisaki and Matsumoto et al. with such a memory array. Without such a reference and motivation, Applicants respectfully submit that the rejections against independent Claim 36 and its dependent claims are improper.

V. Conclusion

In view of the above remarks, Applicants respectfully submit that this application is in condition for allowance. Reconsideration is respectfully requested. If there are any questions concerning this Amendment, the Examiner is invited to contact the undersigned attorney at (312) 321-4719.

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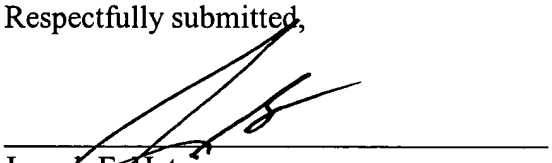
Respectfully submitted,



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